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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Paul A. LaBerge — Attorney Docket No.: 501127.02

Patent No. : US 6,888,760 B2

Issued : May 3, 2005

Title : SYSTEM AND METHOD FOR MULTIPLEXING DATA AND DATA MASKING INFORMATION ON A DATA BUS OF A MEMORY DEVICE

NOTIFICATION OF ERRORS

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

The following errors were noted in a review of the above-identified letters patent. One or more of these errors was inadvertently made in the original application, while the others occurred in the printing of the patent. Since the errors are of an obvious nature, a formal Certificate of Correction is not believed to be warranted at this time. Therefore, applicant requests that this notification be placed in the Patent and Trademark Office file.

Column, Line	Reads	Should Read
Column 1, Line 27	"the chip package"	--to the chip package--
Column 1, Line 50	"coupled to a corresponding data terminals"	--coupled to a corresponding data terminal--
Column 1, Line 65	"increased complexity in informing electrical"	--increased complexity in forming electrical--

Column 2, Line 17	"described a more"	--described in more--
Column 2, Line 19	"more of fewer terminals,"	--more or fewer terminals,--
Column 5, Line 24	"control signals portion"	--control signal portion--
Column 5, Line 29	"signals A**0**-AX signals at positive"	--signals A**0**-AX at positive--
Column 5, Line 34	"which as the same frequency"	--which has the same frequency--
Column 5, Line 56	"to accesses addressed memory cells"	--to access addressed memory cells--
Column 6, Line 2	"and DQS signal"	--and the DQS signal--
Column 6, Line 36	"thereafter applies a data masking"	--thereafter applies data masking--
Column 6, Line 48	"is a merely a write data bits"	--is merely write data bits--
Column 7, Line 41	"transfer the data masking"	--transfer of the data masking--
Column 7, Line 60	"information the mode"	--information on the mode--
Column 8, Line 10	"includes 32 bits,"	--include 32 bits,--
Column 9, Line 11	"further comprising"	--further comprising:--
Column 9, Line 41	"stored in read/write circuit"	--stored in the read/write circuit--
Column 10, Line 3	"stored in read/write circuit"	--stored in the read/write circuit--

Column 10, Lines 57-59	"at least of the data words and to thereafter apply at least one of the masked data word to the memory-cell array."	--at least one of the data words and to thereafter apply at least one of the masked data words to the memory-cell array.--

Respectfully submitted,

Date: Sept. 11, 2007

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Enclosure:
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